Remarks:

Reconsideration of the application is requested.

Claims 1-14 remain in the application. Claim 1 has been amended.

In the second paragraph on page 2 of the above-identified Office action, the Examiner has stated that Fig. 1 is incorrect in depicting region 40 as N type, which should be P type. Appropriate correction has been made.

In the third paragraph on page 2 of the above-identified Office action, claims 1-14 have been rejected as being indefinite under 35 U.S.C. § 112 second paragraph.

More specifically, the Examiner has stated that independent claim 1 is incorrect in reciting "a first doped terminal zone and a second doped terminal zone formed in said insulation layer" and "a drift zone formed in said insulation layer." The Examiner's suggested changes have been made.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. Should the Examiner find any further objectionable items, counsel would appreciate a telephone call during which the matter may be resolved. The above-noted changes to the claims are provided

solely for cosmetic and/or clarificatory reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claims for any reason related to the statutory requirements for a patent.

In the sixth paragraph on page 2 of the above-mentioned Office action, claims 1, 2, 5 and 6 have been rejected as being unpatentable over Letavic et al. (US Pat. No. 6,221,737) together with Assaderaghi et al. (US Pat. No. 6,121,661) under 35 U.S.C. § 103(a).

The rejection has been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 17, line 18 of the specification.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> an insulation layer on said semiconductor substrate, said insulating layer having a thickness of between 50 nm and 200 nm;
>
> .....
>
> at least one of said first doped terminal zone and said second doped terminal zone directly adjoining said semiconductor substrate. (Emphasis added by Applicants.)

The basic structure of the semiconductor component according to the invention of the instant application, i.e. the semiconductor substrate and the insulation layer applied thereon, is a structure with a thin insulation layer which so far has only been used for logic components (for example CMOS transistors), but not for power components with a dielectric strength of more than 10 V. It is noted that SOI substrates for logic components and SOI substrates for power components are different. In SOI substrates for logic components, the insulation layer is much thinner in comparison to the insulation layer in SOI substrates for power semiconductor components, which results in a low dielectric strength of this insulation layer which is just high enough that the lower voltages arising in logic components, normally between 3.3 V and 5V, are tolerated. Furthermore, logic components do not have a drift zone. Such drift zones are only required for power components, in order to achieve a high dielectric strength, whereby the major part of the voltage in such power components drops over the commonly low-doped drift zone. In order to ensure a sufficient dielectric strength for power components on an SOI substrate, the insulation layer must be of sufficient thickness for these SOI substrates.

An SOI component with such a thin insulation layer, a drift zone embodied between a first and a second terminal zone in a semiconductor layer above the insulation layer and a direct

connection of the first or second terminal zone to the semiconductor substrate, is not obvious for a person of skill in the art in view of the prior art references Letavic et al. and Assederaghi et al.

Letavic et al. describe high voltage-sustaining SOI components, where a high voltage- and current-sustaining capability must be ensured (see col. 1, line 10). This can also be seen from the acknowledgement of the state of the art in col. 1 of Letavic et al., in which the importance of the high breakdown voltage of the components is repeatedly emphasized (see col. 1, line 33, lines 52 to 53 and line 64). A basic requirement for a high dielectric strength is an insulation layer with a thickness of between 100 and 5000 nm, preferably between 2000 and 3000 nm according to Letavic et al. (see col. 4, lines 1 to 3), and is thus at least 10 times as thick as the insulation layer in the semiconductor component according to the invention of the instant application.

Letavic et al. contain no hint for a person skilled in the art to reduce the thickness of the insulation layer, because according to the state of art prior to the filing date of the instant application, an insulation layer with such a thickness was indeed required for achieving high voltage-sustaining capabilities.

The semiconductor component according to the invention of the instant application differs from the component according to Assaderaghi et al. in that a drift zone is present in the semiconductor component according to the invention of the instant application, which is not present in the component according to Assaderaghi et al. Assaderaghi et al. describe a circuit with CMOS components, i.e. pure logic components which do not require a drift path, because drift paths are only required for achieving high voltage-sustaining capabilities in power components. Prior to the filing date of the instant application, a person skilled in the art would not have any reason to provide such a drift zone for the CMOS components according to Assederaghi et al., because it must be assumed that voltage-sustaining capabilities, for which a drift zone is necessary, cannot be achieved because of the thin insulation layer in SOI logic components.

The object of the invention of the instant application was to realize power components with higher voltage-sustaining capabilities than the voltage-sustaining capabilities of the thin insulation layer, on SOI substrates with a thin oxide layer which, up until now, had been used exclusively for logic components, and not for power components. This is achieved by the semiconductor component according to the invention of the

instant application in which at least one of the terminal zones is connected immediately to the semiconductor substrate.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

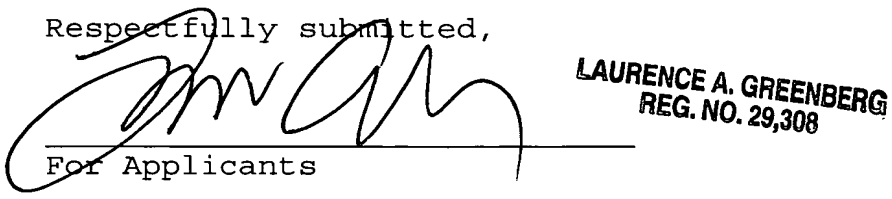
In view of the foregoing, reconsideration and allowance of claims 1-14 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and

Greenberg, P.A., No. 12-1099.

Respectfully submitted,



For Applicants

YHC:cgm

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Marked-Up Version of the Amended Claims:

Claim 1(amended). A semiconductor component, comprising:

a semiconductor substrate;

an insulation layer on said semiconductor substrate, said insulating layer having a thickness of between 50 nm and 200 nm;

a semiconductor layer configured on said insulation layer;

a first doped terminal zone and a second doped terminal zone formed in said [insulation] semiconductor layer; and

a drift zone formed in said [insulation] semiconductor layer;

said drift zone formed between said first doped terminal zone and said second doped terminal zone; and

at least one of said first doped terminal zone and said second doped terminal zone directly adjoining said semiconductor substrate.